Camera Link Technology Brief

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Introduction

The Camera Link Standard

Camera Link is a communications interface developed for use in vision applications. The specification for the Camera Link interface was defined by a group of industrial camera and frame grabber manufacturers. The Camera Link specification is an open specification which gives manufacturers the ability to differentiate their products while maintaining interface compatibility.

In the past, the industrial digital video market has lacked a standard method of communication between cameras and frame grabbers. Camera manufacturers and frame grabber manufacturers developed products with different connectors which made cable integration expensive and very confusing for consumers. Also, as data rates and the complexity of data transmissions continue to increase, the need for a connectivity standard has become critical. In an era of fast, complex data exchange, hand built cables will no longer provide the needed reliability. By specifying a standard pin arrangement and a cable assembly that is specifically designed for reliability at high data rates, the Camera Link standard ensures that compatible devices can be connected with ease. Because the standard specifies readily available chipsets and a cable assembly that is a stock item, customers can take advantage of volume pricing, thus reducing costs. In addition, the existence of a standard interface will decrease the customer's need to spend time getting technical support when integrating a compatible camera and frame grabber.

Technical Description

Many current digital video solutions use LVDS communication as specified for RS-644. While RS-644 LVDS is an improvement over older methods such as RS-422, it still requires bulky cables and has a limited transmission rate. To solve these problems, the Camera Link standard is based on Channel Link® technology developed by National Semiconductor.

Channel Link is the latest advance in LVDS (Low Voltage Differential Signaling) technology for transmitting digital data. Channel Link uses a parallel-to-serial transmitter and a serial-to parallel-receiver to transmit data at rates up to 2.38 Gbps.

As shown in Figure 1, the Channel Link Transmitter converts 28 bits of CMOS/TTL data into four LVDS data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. With each cycle of the transmit clock, 28 bits of input data are sampled and transmitted. The Channel Link receiver converts the data streams back into 28 bits of CMOS/TTL data.

Channel Link technology has several advantages. Since it builds on existing, well understood technologies such as TTL and LVDS, it is easy to learn and implement. Channel Link chip sets are inexpensive and readily available. Also, since it uses low swing differential current mode drivers, Channel Link reduces EMI.

But the major advantage of Channel Link technology is that multiplexing of the data lines provides a substantial cable reduction. With conventional RS-644 technology, transmitting 28 bits of data at a high rate requires 56 conductors just for the data. With Channel Link, as few as 11 conductors (4 data pairs, 1 clock pair and at least one ground) can be used. This results in cables with a smaller form factor and reduced shielding requirements. It also means that smaller connectors can be used on the cables.

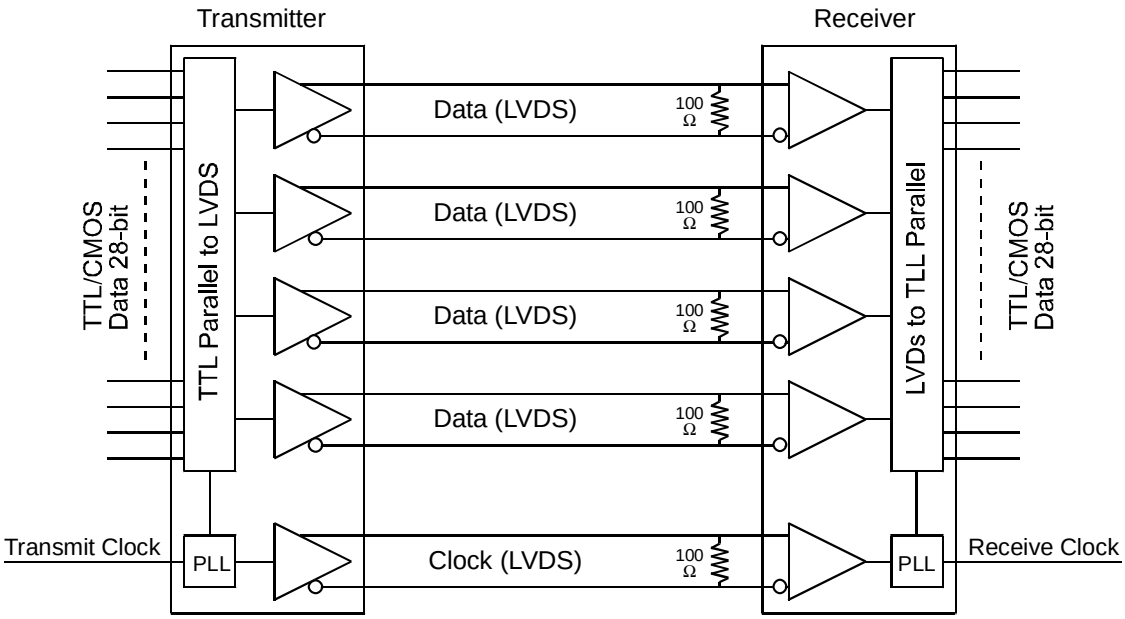

Figure 1: Channel Link Block Diagram

Configurations

The Camera Link interface includes a base configuration, a medium configuration, and a full configuration.

In the base configuration, a single Channel Link transmitter/receiver pair is used along with four RS-644 LVDS pairs reserved for general purpose camera control and two RS-644 LVDS pairs reserved for serial communication between the camera and the frame grabber (see Figure 2).

Since a single Channel Link transmitter/receiver pair is limited to 28 bits of video data, the base configuration may not be adequate for all situations. The medium configuration includes two Channel Link transmitter/receiver pairs along with the LVDS pairs for camera control and serial communication. The medium configuration can transmit up to 56 bits of video data. The full configuration includes three Channel Link transmitter/receiver pairs along with the LVDS pairs for camera control and serial communication. The full configuration can transmit up to 84 bits of video data.

As shown in Figure 2 the base configuration requires one standard cable between the camera and the frame grabber. The medium or the full configuration requires two standard cables between the camera and the frame grabber.

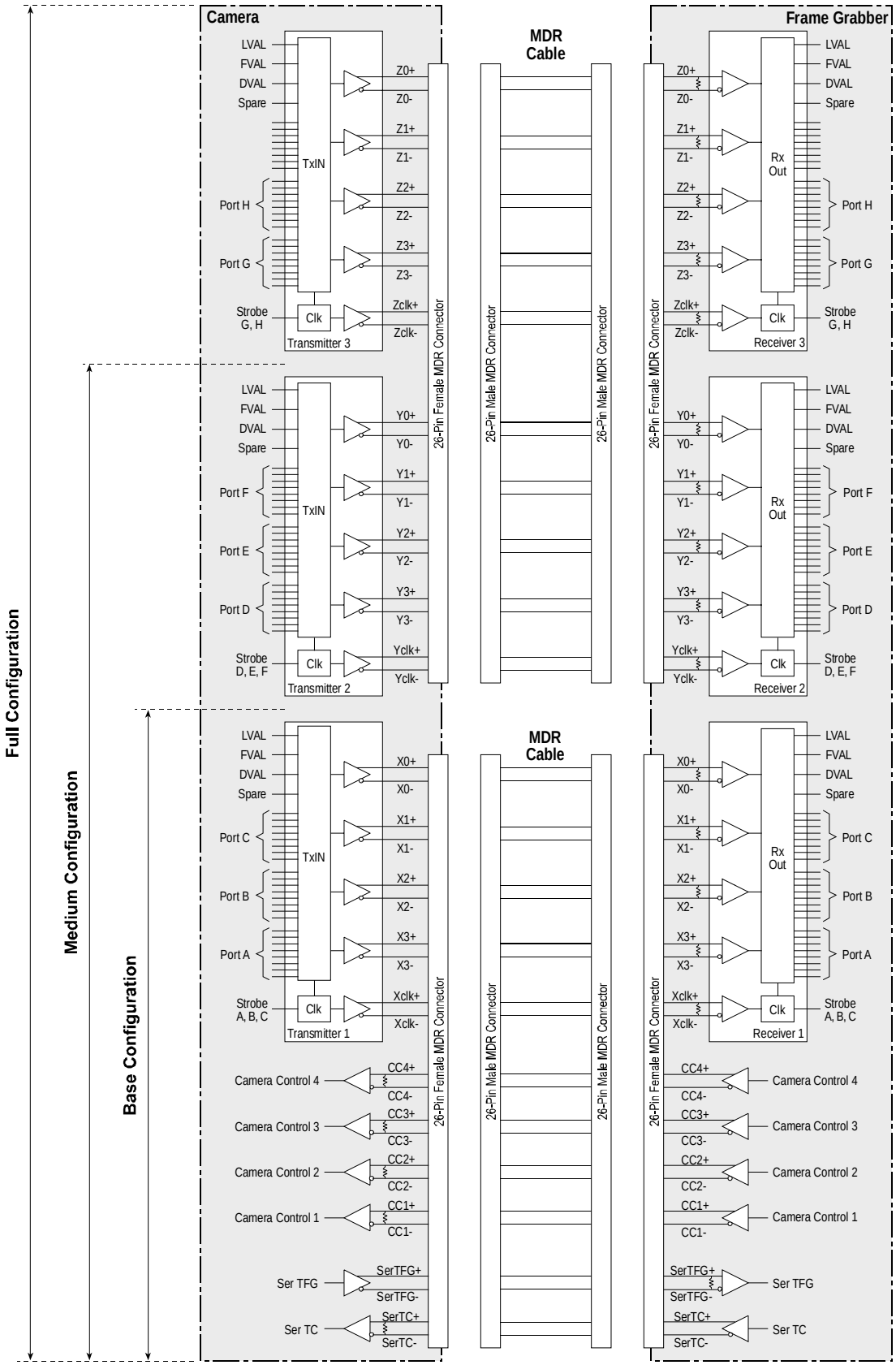

Figure 2: Camera Link Block Diagram

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Camera Signals

Camera signal requirements are divided into four categories:

- Camera Control Signals
- Video Data
- Power
- Serial Communication

Camera Control Signals

In all configurations, four RS-644 LVDS pairs are included for general purpose camera control. Camera manufacturers are free to define these signals to meet the needs of their particular product. These signals are defined as frame grabber outputs and camera inputs. The generic names for the signals are: Camera Control 1 (CC1), Camera Control 2 (CC2), Camera Control 3 (CC3), and Camera Control 4 (CC4).

Basler has chosen the signal definitions shown in Table 1 as its standard. As new functions are added to Basler cameras, new definitions may be added to the table.

Table 1: Camera Control Signal Usage

Generic Signal Name	Short Form	Basler Usage
Camera Control 1	CC1	EXSYNC (external synchronization signal) A transition in this signal causes readout to begin. Some cameras offer modes where the integration time is encoded into the low time or the length of the EXSYNC signal.
Camera Control 2	CC2	Reserved for future use
Camera Control 3	CC3	Reserved for future use
Camera Control 4	CC4	Reserved for future use

Video Data

The Camera Link standard defines four pixel qualifier signal names and describes their signal level. The transmitter/receiver pin assignment and the connector pinout for these signals is fixed by the camera link standard. Table 2 shows the pixel qualifier names and definitions as established by the Channel Link standard. Basler cameras follow the standard for these signals.

Table 2: Pixel Qualifier Signal Descriptions

Signal Name	Short Form	Basler Usage
Frame Valid	FVAL	In area scan cameras, Frame Valid is high or 1 for valid lines. In line scan cameras this signal is not used.
Line Valid	LVAL	In area scan or line scan cameras, Line Valid is high or 1 for valid pixels.
Data Valid	DVAL	This signal is intended to allow cameras with low data rates to use chips that do not support low strobe frequencies by padding the transmissions with dummy words. Generally, this signal will be high for strobes which contain data of interest. On cameras with sufficient data rates, DVAL is not used.
Spare	Spare	Reserved for future use

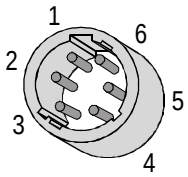
The Camera Link standard also defines Port A through Port H. Ports A through H are logical eight bit words that are used to specify how image data bits are assigned to the transmitter/receiver pins. For more information on image data bit allocations, see Section 3, *Ports and Port Definitions* and Section 4, *Bit Assignments*.

Power

Power is not provided to the camera through the Camera Link connector. Power is supplied to the camera via a separate connector. The standard leaves each camera manufacturer free to define their own power connector, current, and voltage requirements.

Basler will use a Hirose 6 pin receptacle (part number HR10-7R-6PA) on its Camera Link compatible cameras. The receptacle pin numbering and the pin assignments are shown below.

The mating connector to be used on the end of the power cable is the Hirose 6 pin plug (part number HR10-7P-6S)



Hirose 6-pin Receptacle
(as viewed from camera back)

Pin	Assignment
1	+12 VDC
2	+12 VDC
3	Not connected
4	Not connected
5	Gnd
6	Gnd

Serial Communication

In all configurations, two RS-644 LVDS pairs are allocated for asynchronous serial communication between the camera and the frame grabber. Cameras and frame grabbers should be designed to support at least 9600 baud serial communication. The Camera Link standard designates the serial signals as:

SerTFG (LVDS pair for serial communication from the camera to the frame grabber)

SerTC (LVDS pair for serial communication from the frame grabber to the camera)

The serial interface must have the following characteristics: one start bit, one stop bit, no parity, and no handshaking.

The Camera Link standard provides recommended guidelines for camera manufacturers and frame grabber manufacturers to follow when designing a method for accessing and using the asynchronous serial port. The camera configuration utility supplied by Basler will follow the guidelines in the standard.

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Ports and Port Assignments

Port Definition

A port is defined as an eight bit word. The least significant bit (LSB) is bit 0 and the most significant bit (MSB) is bit 7. The Camera Link standard uses eight ports, Port A through Port H.

Port Assignments

In the base configuration, Ports A, B, and C are assigned to the single Channel Link transmitter/receiver pair used in this configuration. In the medium configuration, Ports A, B, and C are assigned to the first transmitter/receiver pair and Ports D, E, and F are assigned to the second transmitter/receiver pair. In the full configuration, Ports A, B, and C are assigned to the first transmitter/receiver pair, Ports D, E, and F are assigned to the second transmitter/receiver pair, and Ports G and H are assigned to the third transmitter/receiver pair (see Figure 2).

Each Channel Link transmitter has 28 data input pins labeled TX0 through TX27. The corresponding receiver has 28 data output pins labeled RX0 through RX27. Table 3 shows how the ports and the timing signals are assigned to the pins on each transmitter/receiver pair.

Table 3: Port Assignments

Full Configuration					
Medium Configuration					
Base Configuration					
Input Name	**Trans/Rec Pair 1 Pin Number**	**Input Name**	**Trans/Rec Pair 2 Pin Number**	**Input Name**	**Trans/Rec Pair 3 Pin Number**
Strobe	TxClkIn/RxClkOut	Strobe	TxClkIn/RxClkOut	Strobe	TxClkIn/RxClkOut
LVAL	TX24/RX24	LVAL	TX24/RX24	LVAL	TX24/RX24
FVAL	TX25/RX25	FVAL	TX25/RX25	FVAL	TX25/RX25
DVAL	TX26/RX26	DVAL	TX26/RX26	DVAL	TX26/RX26
Spare	TX23/RX23	Spare	TX23/RX23	Spare	TX23/RX23
Port A0	TX0/RX0	Port D0	TX0/RX0	Port G0	TX0/RX0
Port A1	TX1/RX1	Port D1	TX1/RX1	Port G1	TX1/RX1
Port A2	TX2/RX2	Port D2	TX2/RX2	Port G2	TX2/RX2
Port A3	TX3/RX3	Port D3	TX3/RX3	Port G3	TX3/RX3
Port A4	TX4/RX4	Port D4	TX4/RX4	Port G4	TX4/RX4
Port A5	TX6/RX6	Port D5	TX6/RX6	Port G5	TX6/RX6
Port A6	TX27/RX27	Port D6	TX27/RX27	Port G6	TX27/RX27
Port A7	TX5/RX5	Port D7	TX5/RX5	Port G7	TX5/RX5
Port B0	TX7/RX7	Port E0	TX7/RX7	Port H0	TX7/RX7
Port B1	TX8/RX8	Port E1	TX8/RX8	Port H1	TX8/RX8
Port B2	TX9/RX9	Port E2	TX9/RX9	Port H2	TX9/RX9
Port B3	TX12/RX12	Port E3	TX12/RX12	Port H3	TX12/RX12
Port B4	TX13/RX13	Port E4	TX13/RX13	Port H4	TX13/RX13
Port B5	TX14/RX14	Port E5	TX14/RX14	Port H5	TX14/RX14
Port B6	TX10/RX10	Port E6	TX10/RX10	Port H6	TX10/RX10
Port B7	TX11/RX11	Port E7	TX11/RX11	Port H7	TX11/RX11
Port C0	TX15/RX15	Port F0	TX15/RX15		
Port C1	TX18/RX18	Port F1	TX18/RX18		
Port C2	TX19/RX19	Port F2	TX19/RX19		
Port C3	TX20/RX20	Port F3	TX20/RX20		
Port C4	TX21/RX21	Port F4	TX21/RX21		
Port C5	TX22/RX22	Port F5	TX22/RX22		
Port C6	TX16/RX16	Port F6	TX16/RX16		
Port C7	TX17/RX17	Port F7	TX17/RX17		

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Bit Assignments

Bit Assignment to Ports

The following tables show how image data bits are assigned to ports for the three Camera Link configurations. The bit assignments have been designed to handle most popular camera output configurations.

Table 4: Image Data Bit to Port Assignments for the Base Configuration

Port	1, 2, or 3 Pixels at 8 Bits/Pixel[1]	1 or 2 Pixels at 10 Bits/Pixel[2]	1 or 2 Pixels at 12 Bits/Pixel[2]	1 Pixel at 14 Bits/Pixel	1 Pixel at 16 Bits/Pixel	24 Bit RGB
Port A0	Pixel A Bit 0	Pixel A Bit 0	Pixel A Bit 0	Pixel A Bit 0	Pixel A Bit 0	Red Bit 0
Port A1	Pixel A Bit 1	Pixel A Bit 1	Pixel A Bit 1	Pixel A Bit 1	Pixel A Bit 1	Red Bit 1
Port A2	Pixel A Bit 2	Pixel A Bit 2	Pixel A Bit 2	Pixel A Bit 2	Pixel A Bit 2	Red Bit 2
Port A3	Pixel A Bit 3	Pixel A Bit 3	Pixel A Bit 3	Pixel A Bit 3	Pixel A Bit 3	Red Bit 3
Port A4	Pixel A Bit 4	Pixel A Bit 4	Pixel A Bit 4	Pixel A Bit 4	Pixel A Bit 4	Red Bit 4
Port A5	Pixel A Bit 5	Pixel A Bit 5	Pixel A Bit 5	Pixel A Bit 5	Pixel A Bit 5	Red Bit 5
Port A6	Pixel A Bit 6	Pixel A Bit 6	Pixel A Bit 6	Pixel A Bit 6	Pixel A Bit 6	Red Bit 6
Port A7	Pixel A Bit 7	Pixel A Bit 7	Pixel A Bit 7	Pixel A Bit 7	Pixel A Bit 7	Red Bit 7
Port B0	Pixel B Bit 0	Pixel A Bit 8	Pixel A Bit 8	Pixel A Bit 8	Pixel A Bit 8	Green Bit 0
Port B1	Pixel B Bit 1	Pixel A Bit 9	Pixel A Bit 9	Pixel A Bit 9	Pixel A Bit 9	Green Bit 1
Port B2	Pixel B Bit 2	Not assigned	Pixel A Bit 10	Pixel A Bit 10	Pixel A Bit 10	Green Bit 2
Port B3	Pixel B Bit 3	Not assigned	Pixel A Bit 11	Pixel A Bit 11	Pixel A Bit 11	Green Bit 3
Port B4	Pixel B Bit 4	Pixel B Bit 8	Pixel B Bit 8	Pixel A Bit 12	Pixel A Bit 12	Green Bit 4
Port B5	Pixel B Bit 5	Pixel B Bit 9	Pixel B Bit 9	Pixel A Bit 13	Pixel A Bit 13	Green Bit 5
Port B6	Pixel B Bit 6	Not assigned	Pixel B Bit 10	Not assigned	Pixel A Bit 14	Green Bit 6
Port B7	Pixel B Bit 7	Not assigned	Pixel B Bit 11	Not assigned	Pixel A Bit 15	Green Bit 7
Port C0	Pixel C Bit 0	Pixel B Bit 0	Pixel B Bit 0	Not assigned	Not assigned	Blue Bit 0
Port C1	Pixel C Bit 1	Pixel B Bit 1	Pixel B Bit 1	Not assigned	Not assigned	Blue Bit 1
Port C2	Pixel C Bit 2	Pixel B Bit 2	Pixel B Bit 2	Not assigned	Not assigned	Blue Bit 2
Port C3	Pixel C Bit 3	Pixel B Bit 3	Pixel B Bit 3	Not assigned	Not assigned	Blue Bit 3
Port C4	Pixel C Bit 4	Pixel B Bit 4	Pixel B Bit 4	Not assigned	Not assigned	Blue Bit 4
Port C5	Pixel C Bit 5	Pixel B Bit 5	Pixel B Bit 5	Not assigned	Not assigned	Blue Bit 5
Port C6	Pixel C Bit 6	Pixel B Bit 6	Pixel B Bit 6	Not assigned	Not assigned	Blue Bit 6
Port C7	Pixel C Bit 7	Pixel B Bit 7	Pixel B Bit 7	Not assigned	Not assigned	Blue Bit 7

[1] If the camera is outputting only one pixel per cycle, the port assignments for Pixel A are used. If the camera is outputting two pixels, the port assignments for Pixel A and Pixel for B are used. If the camera is outputting three pixels, the port assignments for Pixel A, for Pixel B, and Pixel for C are used.

[2] If the camera is outputting only one pixel per cycle, the port assignments for Pixel A are used. If the camera is outputting two pixels, the port assignments for Pixel A and for Pixel B are used.

Table 5: Image Data Bit to Port Assignments for the Medium Configuration

Port	4 Pixels at 8 Bits/Pixel	3 or4 Pixels at 10 Bits/Pixel	3 or 4 Pixels at 12 Bits/Pixel	30 Bit RGB	36 Bit RGB
Port A0	Pixel A Bit 0	Pixel A Bit 0	Pixel A Bit 0	Red Bit 0	Red Bit 0
Port A1	Pixel A Bit 1	Pixel A Bit 1	Pixel A Bit 1	Red Bit 1	Red Bit 1
Port A2	Pixel A Bit 2	Pixel A Bit 2	Pixel A Bit 2	Red Bit 2	Red Bit 2
Port A3	Pixel A Bit 3	Pixel A Bit 3	Pixel A Bit 3	Red Bit 3	Red Bit 3
Port A4	Pixel A Bit 4	Pixel A Bit 4	Pixel A Bit 4	Red Bit 4	Red Bit 4
Port A5	Pixel A Bit 5	Pixel A Bit 5	Pixel A Bit 5	Red Bit 5	Red Bit 5
Port A6	Pixel A Bit 6	Pixel A Bit 6	Pixel A Bit 6	Red Bit 6	Red Bit 6
Port A7	Pixel A Bit 7	Pixel A Bit 7	Pixel A Bit 7	Red Bit 7	Red Bit 7
Port B0	Pixel B Bit 0	Pixel A Bit 8	Pixel A Bit 8	Red Bit 8	Red Bit 8
Port B1	Pixel B Bit 1	Pixel A Bit 9	Pixel A Bit 9	Red Bit 9	Red Bit 9
Port B2	Pixel B Bit 2	Not assigned	Pixel A Bit 10	Not assigned	Red Bit 10
Port B3	Pixel B Bit 3	Not assigned	Pixel A Bit 11	Not assigned	Red Bit 11
Port B4	Pixel B Bit 4	Pixel B Bit 8	Pixel B Bit 8	Blue Bit 8	Blue Bit 8
Port B5	Pixel B Bit 5	Pixel B Bit 9	Pixel B Bit 9	Blue Bit 9	Blue Bit 9
Port B6	Pixel B Bit 6	Not assigned	Pixel B Bit 10	Not assigned	Blue Bit 10
Port B7	Pixel B Bit 7	Not assigned	Pixel B Bit 11	Not assigned	Blue Bit 11
Port C0	Pixel C Bit 0	Pixel B Bit 0	Pixel B Bit 0	Blue Bit 0	Blue Bit 0
Port C1	Pixel C Bit 1	Pixel B Bit 1	Pixel B Bit 1	Blue Bit 1	Blue Bit 1
Port C2	Pixel C Bit 2	Pixel B Bit 2	Pixel B Bit 2	Blue Bit 2	Blue Bit 2
Port C3	Pixel C Bit 3	Pixel B Bit 3	Pixel B Bit 3	Blue Bit 3	Blue Bit 3
Port C4	Pixel C Bit 4	Pixel B Bit 4	Pixel B Bit 4	Blue Bit 4	Blue Bit 4
Port C5	Pixel C Bit 5	Pixel B Bit 5	Pixel B Bit 5	Blue Bit 5	Blue Bit 5
Port C6	Pixel C Bit 6	Pixel B Bit 6	Pixel B Bit 6	Blue Bit 6	Blue Bit 6
Port C7	Pixel C Bit 7	Pixel B Bit 7	Pixel B Bit 7	Blue Bit 7	Blue Bit 7
Port D0	Pixel D Bit 0	Pixel D Bit 0	Pixel D Bit 0	Not assigned	Not assigned
Port D1	Pixel D Bit 1	Pixel D Bit 1	Pixel D Bit 1	Not assigned	Not assigned
Port D2	Pixel D Bit 2	Pixel D Bit 2	Pixel D Bit 2	Not assigned	Not assigned
Port D3	Pixel D Bit 3	Pixel D Bit 3	Pixel D Bit 3	Not assigned	Not assigned
Port D4	Pixel D Bit 4	Pixel D Bit 4	Pixel D Bit 4	Not assigned	Not assigned
Port D5	Pixel D Bit 5	Pixel D Bit 5	Pixel D Bit 5	Not assigned	Not assigned
Port D6	Pixel D Bit 6	Pixel D Bit 6	Pixel D Bit 6	Not assigned	Not assigned
Port D7	Pixel D Bit 7	Pixel D Bit 7	Pixel D Bit 7	Not assigned	Not assigned
Port E0	Not assigned	Pixel C Bit 0	Pixel C Bit 0	Green Bit 0	Green Bit 0
Port E1	Not assigned	Pixel C Bit 1	Pixel C Bit 1	Green Bit 1	Green Bit 1
Port E2	Not assigned	Pixel C Bit 2	Pixel C Bit 2	Green Bit 2	Green Bit 2
Port E3	Not assigned	Pixel C Bit 3	Pixel C Bit 3	Green Bit 3	Green Bit 3
Port E4	Not assigned	Pixel C Bit 4	Pixel C Bit 4	Green Bit 4	Green Bit 4
Port E5	Not assigned	Pixel C Bit 5	Pixel C Bit 5	Green Bit 5	Green Bit 5
Port E6	Not assigned	Pixel C Bit 6	Pixel C Bit 6	Green Bit 6	Green Bit 6
Port E7	Not assigned	Pixel C Bit 7	Pixel C Bit 7	Green Bit 7	Green Bit 7
Port F0	Not assigned	Pixel C Bit 8	Pixel C Bit 8	Green Bit 8	Green Bit 8
Port F1	Not assigned	Pixel C Bit 9	Pixel C Bit 9	Green Bit 9	Green Bit 9
Port F2	Not assigned	Not assigned	Pixel C Bit 10	Not assigned	Green Bit 10
Port F3	Not assigned	Not assigned	Pixel C Bit 11	Not assigned	Green Bit 11
Port F4	Not assigned	Pixel D Bit 8	Pixel D Bit 8	Not assigned	Not assigned
Port F5	Not assigned	Pixel D Bit 9	Pixel D Bit 9	Not assigned	Not assigned
Port F6	Not assigned	Not assigned	Pixel D Bit 10	Not assigned	Not assigned
Port F7	Not assigned	Not assigned	Pixel D Bit 11	Not assigned	Not assigned

Table 6: Image Data Bit to Port Assignments for the Full Configuration

Port	8 Pixels at 8 Bits/Pixel		Port	8 Pixels at 8 Bits/Pixel
Port A0	Pixel A Bit 0		Port E0	Pixel E Bit 0
Port A1	Pixel A Bit 1		Port E1	Pixel E Bit 1
Port A2	Pixel A Bit 2		Port E2	Pixel E Bit 2
Port A3	Pixel A Bit 3		Port E3	Pixel E Bit 3
Port A4	Pixel A Bit 4		Port E4	Pixel E Bit 4
Port A5	Pixel A Bit 5		Port E5	Pixel E Bit 5
Port A6	Pixel A Bit 6		Port E6	Pixel E Bit 6
Port A7	Pixel A Bit 7		Port E7	Pixel E Bit 7
Port B0	Pixel B Bit 0		Port F0	Pixel F Bit 0
Port B1	Pixel B Bit 1		Port F1	Pixel F Bit 1
Port B2	Pixel B Bit 2		Port F2	Pixel F Bit 2
Port B3	Pixel B Bit 3		Port F3	Pixel F Bit 3
Port B4	Pixel B Bit 4		Port F4	Pixel F Bit 4
Port B5	Pixel B Bit 5		Port F5	Pixel F Bit 5
Port B6	Pixel B Bit 6		Port F6	Pixel F Bit 6
Port B7	Pixel B Bit 7		Port F7	Pixel F Bit 7
Port C0	Pixel C Bit 0		Port G0	Pixel G Bit 0
Port C1	Pixel C Bit 1		Port G1	Pixel G Bit 1
Port C2	Pixel C Bit 2		Port G2	Pixel G Bit 2
Port C3	Pixel C Bit 3		Port G3	Pixel G Bit 3
Port C4	Pixel C Bit 4		Port G4	Pixel G Bit 4
Port C5	Pixel C Bit 5		Port G5	Pixel G Bit 5
Port C6	Pixel C Bit 6		Port G6	Pixel G Bit 6
Port C7	Pixel C Bit 7		Port G7	Pixel G Bit 7
Port D0	Pixel D Bit 0		Port H0	Pixel H Bit 0
Port D1	Pixel D Bit 1		Port H1	Pixel H Bit 1
Port D2	Pixel D Bit 2		Port H2	Pixel H Bit 2
Port D3	Pixel D Bit 3		Port H3	Pixel H Bit 3
Port D4	Pixel D Bit 4		Port H4	Pixel H Bit 4
Port D5	Pixel D Bit 5		Port H5	Pixel H Bit 5
Port D6	Pixel D Bit 6		Port H6	Pixel H Bit 6
Port D7	Pixel D Bit 7		Port H7	Pixel H Bit 7

5 Connectors, Cables, and Pinouts

The high-frequency transfer rates of Channel Link make connector and cable selection critical. Compliance with the cable, connector, and pinout specifications in the Camera Link standard is essential for successful camera and frame grabber operation.

Connectors

The 3M 26-pin MDR (Mini D Ribbon) connector was selected for use with Camera Link due to its robust design and previous successful experience with the high-frequency transfer rates of Channel Link. 3M corporation has worked closely with National Semiconductor to test and define the performance of the MDR products for use with Channel Link chipsets. Board mount MDR connectors are available in a variety of configurations including vertical and right-angle through hole as well as right-angle surface mount.

Table 7 shows the part numbers for some of the currently available 3M connectors.

Jacksockets should be used when mounting one of these connectors on a camera or a frame grabber. Jacksockets will make the connectors compatible with the thumbscrews on the standard Camera Link cable.

Table 7: Recommended Connectors

3M Part Number	Connector Description
10226-2200VE	Vertical, SMT
10226-1A10VE	Right Angle, SMT
10226-6212VC	Vertical, Through-hole
10226-55G3VC	Right Angle, Through-hole

Cables

3M has also designed a cable assembly specifically for use with cameras and frame grabbers complying with the Camera Link standard. The twin-ax shielded cable used in the cable assembly meets all of the stringent demands for reliable high-speed differential signaling applications. The 3M part number for the cable is 14X26-SZLB-XXX-0LC. The cable is available in lengths from one meter to ten meters and with two different shell options. Each shell includes thumbscrews for positive retention.

Pinouts

Table 8 shows the pin assignments for the 26-pin MDR connectors on the camera and on the frame grabber. Figure 3 shows the pin assignments for the base configuration in a graphical fashion.

Table 8: Pin Assignments

Medium and Full Configuration (One or Two Additional Channel Link Chipsets)				Base Configuration (One Channel Link Chipset + Camera Control + Serial Communication)		
Camera Connector Pin #	Frame Grabber Connector Pin #	Channel Link Signal	Cable Name (Reference only)	Camera Connector Pin #	Frame Grabber Connector Pin #	Channel Link Signal
1	1	Inner Shield	Inner Shield	1	1	Inner Shield
14	14	Inner Shield	Inner Shield	14	14	Inner Shield
2	25	Y0-	Pair 1-	2	25	X0-
15	12	Y0+	Pair 1+	15	12	X0+
3	24	Y1-	Pair 2-	3	24	X1-
16	11	Y1+	Pair 2+	16	11	X1+
4	23	Y2-	Pair 3-	4	23	X2-
17	10	Y2+	Pair 3+	17	10	X2+
5	22	Yclk-	Pair 4-	5	22	Xclk-
18	9	Yclk+	Pair 4+	18	9	Xclk+
6	21	Y3-	Pair 5-	6	21	X3-
19	8	Y3+	Pair 5+	19	8	X3+
7	20	100 Ohm	Pair 6+	7	20	SerTC+
20	7	Terminated	Pair 6-	20	7	SerTC-
8	19	Z0-	Pair 7-	8	19	SerTFG-
21	6	Z0+	Pair 7+	21	6	SerTFG+
9	18	Z1-	Pair 8-	9	18	CC1-
22	5	Z1+	Pair 8+	22	5	CC1+
10	17	Z2-	Pair 9+	10	17	CC2+
23	4	Z2+	Pair 9-	23	4	CC2-
11	16	Zclk-	Pair 10-	11	16	CC3-
24	3	Zclk+	Pair 10+	24	3	CC3+
12	15	Z3-	Pair 11+	12	15	CC4+
25	2	Z3+	Pair 11-	25	2	CC4-
13	13	Inner Shield	Inner Shield	13	13	Inner Shield
26	26	Inner Shield	Inner Shield	26	26	Inner Shield

Shielding

The Camera Link Standard recommends that the inner shields be tied to digital ground in cameras and Basler will follow this recommendation. The standard also recommends that in frame grabbers, the inner shields be tied to digital ground through a zero ohm resistor. This will allow the resistor to be removed in the field and replaced with a high-value resistor and a parallel capacitor if necessary to prevent ground loops.

Unused pairs should be terminated to 100 ohms at each end.

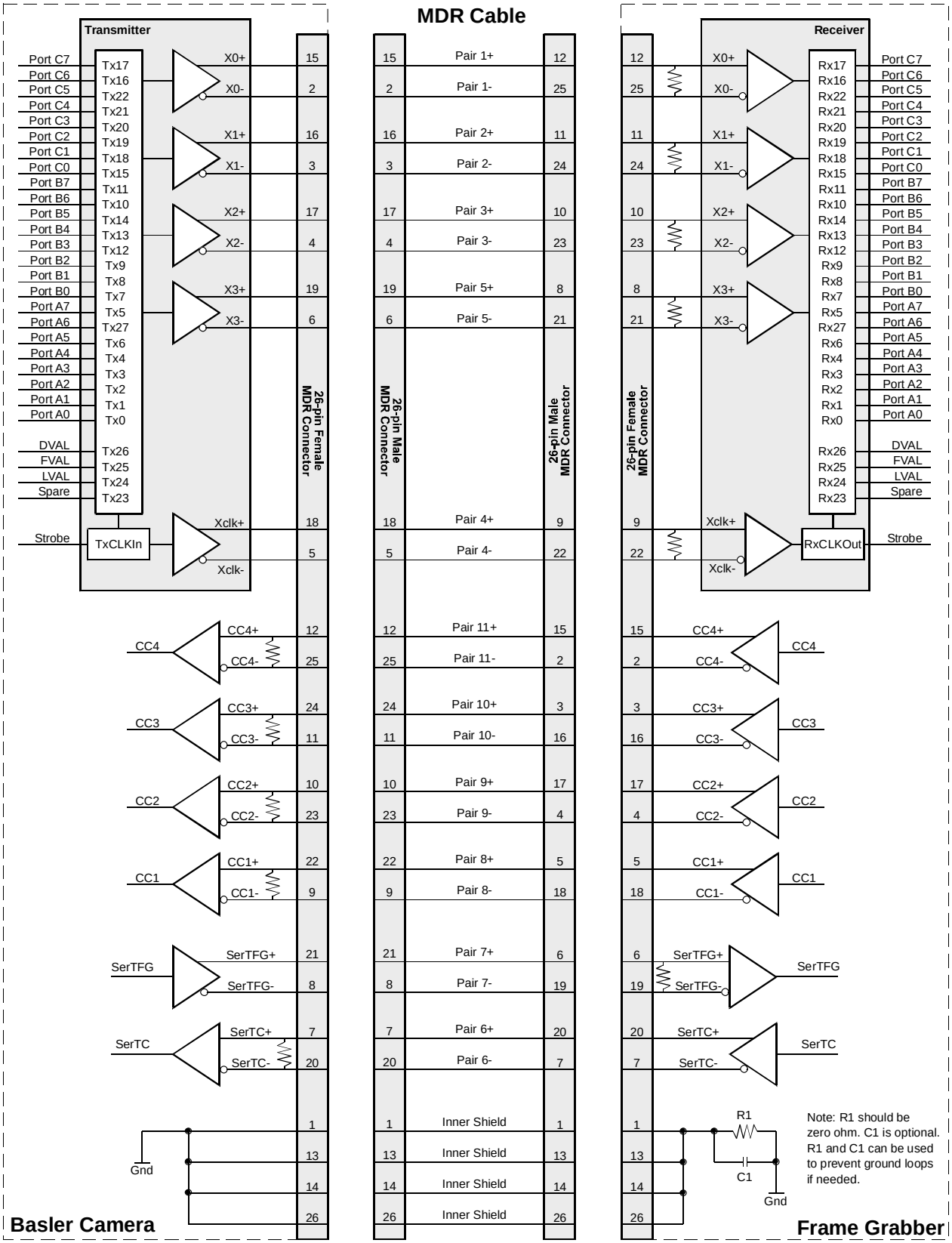

Figure 3: Camera and Frame Grabber Pin Assignments (Base Configuration)

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Chipsets

Standard Chipsets

The Camera Link standard specifies that transmission of video data will be handled by 28-bit Channel Link chips manufactured by National Semiconductor. Table 9 lists some of the current National Semiconductor transmitter and receiver sets that will inter-operate. Detailed data sheets for these parts are available at the National Semiconductor web site: www.national.com.

Basler cameras will use chips that are compatible with the standard.

Due to potential interface issues, chipsets using technology similar to Channel Link (such as Flatlink® by Texas Instruments and Panel Link® by Silicon Image) are not considered compatible with the Camera Link standard.

Table 9: Channel Link Chipsets Compatible with Camera Link

National Semiconductor Product Number	Function	Supply Voltage	Speed
DS90CR281	Transmitter	5 V	20-40 MHz
DS90CR282	Receiver	5 V	20-40 MHz
DS90CR283	Transmitter	5 V	20-66 MHz
DS90CR284	Receiver	5 V	20-66 MHz
DS90CR285	Transmitter	3.3 V	20-66 MHz
DS90CR286	Receiver	3.3 V	20-66 MHz
DS90CR286A	Receiver	3.3 V	20-66 MHz
DS90CR287	Transmitter	3.3 V	20-85 MHz
DS90CR288	Receiver	3.3 V	20-75 MHz
DS90CR288A	Receiver	3.3 V	20-85 MHz

The recommended National Semiconductor driver/receiver chipset for camera control signals is:

DS90LV047	Transmitter	3.3 V
DS90LV048	Receiver	3.3V